第 81 回ナノ・スピン工学研究会開催のご案内

日　時：　2015 年 11 月 12 日（木）10:00～11:00

場　所：　電気通信研究所　ナノ・スピン総合研究棟 4 階 401 号室(A401)

講演者：　Prof. Jordi Madrenas (Technical University of Catalunya)

講演題目：　"Efficient Emulation of Spiking Neural Networks with SIMD and pipeline serial AER mapped on FPGAs"

講演概要：

After a brief introduction of the mixed-signal design AHA research group at UPC (Technical University of Catalunya, Barcelona, Spain), which includes different CMOS techniques, such as integrated MEMS, translinear FPAA, min-max circuits and other blocks, the main topic of the speech is presented.

The efficient emulation of complex Spiking Neural Networks (SNNs) presents two main challenges: a) Massive parallelism of neurons and synapses; b) Complex connectivity among them.

In order to efficiently emulate neurons and synapses, a parallel multiprocessor architecture based on simple custom processors operating on a Single-Instruction Multiple-Data (SIMD) basis is proposed. The main properties of such architecture, namely, software-programmable algorithms, parallel emulation of neural parameters, serial emulation of synapses and local parameter memory, support any spiking model and real-time execution with excellent scalability.

To cope with the interconnect complexity, a serial pipelined ring topology based on Address Event Representation (AER) is proposed. The AER transmission allows channel multiplexing while still providing real-time operation, due to the low-frequency of biological spikes. The serial ring topology presents a much better scalability than parallel or serial common buses, because it only uses local, point-to-point lines.

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